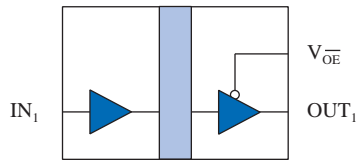


## High Speed/High Temperature Digital Isolators

### Functional Diagram



**IL710**

### Truth Table

$V_I$	$V_{OE}$	$V_O$
L	L	L
H	L	H
L	H	Z
H	H	Z

### Features

- +5 V/+3.3 V CMOS / TTL Compatible
- High Speed: 150 Mbps Typical (IL710S)
- High Temperature:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  (IL710T)
- 2500  $V_{\text{RMS}}$  Isolation (1 min.)
- 300 ps Typical Pulse Width Distortion (IL710S)
- 4 ns Typical Propagation Delay Skew
- 10 ns Typical Propagation Delay
- 30 kV/ $\mu\text{s}$  Typical Common Mode Transient Immunity
- 8-pin MSOP, SOIC, and PDIP Packages
- UL1577 and IEC 61010-2001 Approval

### Applications

- Digital Fieldbus
- RS-485 and RS-422
- Multiplexed Data Transmission
- Data Interfaces
- Board-to-Board Communication
- Digital Noise Reduction
- Operator Interface
- Ground Loop Elimination
- Peripheral Interfaces
- Serial Communication
- Logic Level Shifting

### Description

NVE's IL700 family of high-speed digital isolators are CMOS devices manufactured with NVE's patented\* IsoLoop<sup>®</sup> spintronic Giant Magnetoresistive (GMR) technology. The IL710S is the world's fastest isolator of its type, with a 150 Mbps typical data rate.

The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion as low as 300 ps (0.3 ns), achieving the best specifications of any isolator. Typical transient immunity of 30 kV/ $\mu\text{s}$  is unsurpassed. The IL710 is ideal for isolating applications such as PROFIBUS, RS-485, and RS422.

The IL710 is available in 8-pin MSOP, SOIC, and PDIP packages. Standard and S-Grade parts are specified over a temperature range of  $-40^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$ ; T-Grade parts are specified over a temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

## Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	$T_s$	-55		150	°C	
Ambient Operating Temperature <sup>(1)</sup> IL710T	$T_A$	-55		125 135	°C	
Supply Voltage	$V_{DD1}, V_{DD2}$	-0.5		7	V	
Input Voltage	$V_I$	-0.5		$V_{DD1}+0.5$	V	
Input Voltage	$V_{OE}$	-0.5		$V_{DD2}+0.5$	V	
Output Voltage	$V_O$	-0.5		$V_{DD2}+0.5$	V	
Output Current Drive	$I_O$			10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

## Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature IL710 and IL710S	$T_A$	-40		100	°C	
IL710T	$T_A$	-40		125	°C	
Supply Voltage	$V_{DD1}, V_{DD2}$	3.0		5.5	V	
Logic High Input Voltage	$V_{IH}$	2.4		$V_{DD1}$	V	
Logic Low Input Voltage	$V_{IL}$	0		0.8	V	
Input Signal Rise and Fall Times	$t_{IR}, t_{IF}$			1	µs	

## Insulation Specifications

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance						
MSOP		3.01			mm	
SOIC		4.04			mm	
PDIP		7.04			mm	
Leakage Current			0.2		µA	240 V <sub>RMS</sub> , 60 Hz
Barrier Impedance			$>10^{14} \parallel 3$		$\Omega \parallel pF$	

## Package Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Capacitance (Input-Output) <sup>(5)</sup>	$C_{I-O}$		1.1		pF	f = 1 MHz
Thermal Resistance						
MSOP	$\theta_{JC}$		168		°C/W	Thermocouple at center underside of package
SOIC	$\theta_{JC}$		144		°C/W	
PDIP	$\theta_{JC}$		54		°C/W	
Package Power Dissipation	$P_{PD}$			150	mW	f = 1 MHz, $V_{DD} = 5 V$

## Safety and Approvals

### IEC61010-1

TUV Certificate Numbers:

N1502812, N1502812-101

### Classification as Reinforced Insulation

Model	Package	Pollution Degree	Material Group	Max. Working Voltage
IL710-1	MSOP		Pending Approval	
IL710-2	PDIP	II	III	300 V <sub>RMS</sub>
IL710-3	SOIC	II	III	150 V <sub>RMS</sub>

### UL 1577

Component Recognition Program File Number: E207481

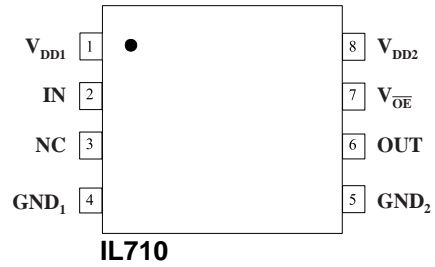
Rated 2500V<sub>RMS</sub> for 1 minute

## Soldering Profile

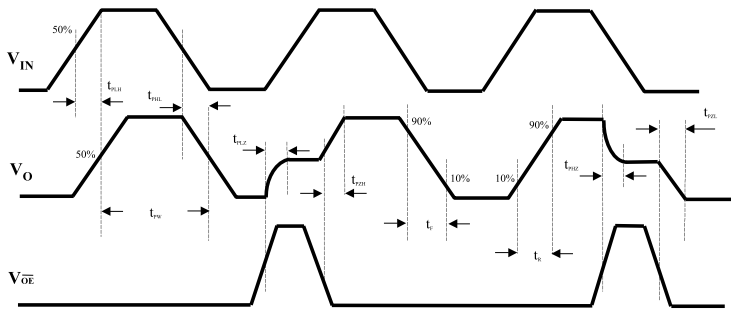
Per JEDEC J-STD-020C, MSL=2

**IL710 Pin Connections**

1	$V_{DD1}$	Supply voltage
2	IN	Data In
3	NC	No internal connection
4	$GND_1$	Ground return for $V_{DD1}$
5	$GND_2$	Ground return for $V_{DD2}$
6	OUT	Data Out
7	$V_{OE}$	Output enable. Internally held low with 100 k $\Omega$
8	$V_{DD2}$	Supply voltage



**Timing Diagram**



**Legend**

$t_{PLH}$	Propagation Delay, Low to High
$t_{PHL}$	Propagation Delay, High to Low
$t_{PW}$	Minimum Pulse Width
$t_{PLZ}$	Propagation Delay, Low to High Impedance
$t_{PZH}$	Propagation Delay, High Impedance to High
$t_{PHZ}$	Propagation Delay, High to High Impedance
$t_{PZL}$	Propagation Delay, High Impedance to Low
$t_R$	Rise Time
$t_F$	Fall Time

### 3.3 Volt Electrical Specifications

Electrical specifications are  $T_{min}$  to  $T_{max}$  unless otherwise stated.

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
<b>DC Specifications</b>						
Input Quiescent Supply Current	$I_{DD1}$		8	10	$\mu\text{A}$	
Output Quiescent Supply Current	$I_{DD2}$		1.7	2	mA	
Logic Input Current	$I_I$	-10		10	$\mu\text{A}$	
Logic High Output Voltage	$V_{OH}$	$V_{DD}-0.1$	$V_{DD}$		V	$I_O = -20 \mu\text{A}, V_I = V_{IH}$
		$0.8 \times V_{DD}$	$0.9 \times V_{DD}$			$I_O = -4 \text{ mA}, V_I = V_{IH}$
Logic Low Output Voltage	$V_{OL}$		0	0.1	V	$I_O = 20 \mu\text{A}, V_I = V_{IL}$
			0.5	0.8		$I_O = 4 \text{ mA}, V_I = V_{IL}$
<b>Switching Specifications</b>						
Maximum Data Rate IL710 and IL710T IL710S		100 130	110 140		Mbps Mbps	$C_L = 15 \text{ pF}$ $C_L = 15 \text{ pF}$
Pulse Width <sup>(7)</sup>	PW	10	7.5		ns	50% Points, $V_o$
Propagation Delay Input to Output (High to Low)	$t_{PHL}$		12	18	ns	$C_L = 15 \text{ pF}$
Propagation Delay Input to Output (Low to High)	$t_{PLH}$		12	18	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High to High Impedance)	$t_{PHZ}$		3	5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (Low to High Impedance)	$t_{PLZ}$		3	5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High Impedance to High)	$t_{PZH}$		3	5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High Impedance to Low)	$t_{PZL}$		3	5	ns	$C_L = 15 \text{ pF}$
Pulse Width Distortion <sup>(2)</sup> IL710 IL710S	PWD		2 1	3 3	ns	$C_L = 15 \text{ pF}$
Propagation Delay Skew <sup>(3)</sup>	$t_{PSK}$		4	6	ns	$C_L = 15 \text{ pF}$
Output Rise Time (10%–90%)	$t_R$		2	4	ns	$C_L = 15 \text{ pF}$
Output Fall Time (10%–90%)	$t_F$		2	4	ns	$C_L = 15 \text{ pF}$
Common Mode Transient Immunity (Output Logic High or Logic Low) <sup>(4)</sup>	$ CM_H ,  CM_L $	20	30		kV/ $\mu\text{s}$	$V_{CM} = 300 \text{ V}$
Dynamic Power Consumption <sup>(6)</sup>			140	240	$\mu\text{A}/\text{MHz}$	

## 5 Volt Electrical Specifications

Electrical specifications are  $T_{min}$  to  $T_{max}$  unless otherwise stated.

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
<b>DC Specifications</b>						
Input Quiescent Supply Current	$I_{DD1}$		10	15	$\mu\text{A}$	
Output Quiescent Supply Current	$I_{DD2}$		2.5	3	mA	
Logic Input Current	$I_I$	-10		10	$\mu\text{A}$	
Logic High Output Voltage	$V_{OH}$	$V_{DD}-0.1$	$V_{DD}$		V	$I_O = -20 \mu\text{A}, V_I = V_{IH}$
		$0.8 \times V_{DD}$	$0.9 \times V_{DD}$			$I_O = -4 \text{ mA}, V_I = V_{IH}$
Logic Low Output Voltage	$V_{OL}$		0	0.1	V	$I_O = 20 \mu\text{A}, V_I = V_{IL}$
			0.5	0.8		$I_O = 4 \text{ mA}, V_I = V_{IL}$
<b>Switching Specifications</b>						
Maximum Data Rate IL710 and IL710T IL710S		100 130	110 150		Mbps Mbps	$C_L = 15 \text{ pF}$ $C_L = 15 \text{ pF}$
Pulse Width <sup>(7)</sup>	PW	10	7.5		ns	50% Points, $V_o$
Propagation Delay Input to Output (High to Low)	$t_{PHL}$		10	15	ns	$C_L = 15 \text{ pF}$
Propagation Delay Input to Output (Low to High)	$t_{PLH}$		10	15	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High to High Impedance)	$t_{PHZ}$		3	5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (Low to High Impedance)	$t_{PLZ}$		3	5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High Impedance to High)	$t_{PZH}$		3	5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High Impedance to Low)	$t_{PZL}$		3	5	ns	$C_L = 15 \text{ pF}$
Pulse Width Distortion <sup>(2)</sup> IL710 IL710S	PWD		2 0.3	3 3	ns	$C_L = 15 \text{ pF}$
Propagation Delay Skew <sup>(3)</sup>	$t_{PSK}$		4	6	ns	$C_L = 15 \text{ pF}$
Output Rise Time (10%–90%)	$t_R$		1	3	ns	$C_L = 15 \text{ pF}$
Output Fall Time (10%–90%)	$t_F$		1	3	ns	$C_L = 15 \text{ pF}$
Common Mode Transient Immunity (Output Logic High or Logic Low) <sup>(4)</sup>	$ CM_H ,  CM_L $	20	30		kV/ $\mu\text{s}$	$V_{cm} = 300 \text{ V}$
Dynamic Power Consumption <sup>(6)</sup>			200	340	$\mu\text{A}/\text{MHz}$	

### Notes (apply to both 3.3 V and 5 V specifications):

- Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
- PWD is defined as  $|t_{PHL} - t_{PLH}|$ . %PWD is equal to PWD divided by pulse width.
- $t_{PSK}$  is the magnitude of the worst-case difference in  $t_{PHL}$  and/or  $t_{PLH}$  between devices at 25°C.
- $CM_H$  is the maximum common mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{DD2}$ .  $CM_L$  is the maximum common mode input voltage that can be sustained while maintaining  $V_o < 0.8 \text{ V}$ . The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
- Device is considered a two terminal device: pins 1–4 shorted and pins 5–8 shorted.
- Dynamic power consumption is calculated per channel and is supplied by the channel's input side power supply.
- Minimum pulse width is the minimum value at which specified PWD is guaranteed.

### Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

## Application Information

### Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

### Power Supply Decoupling

Both power supplies to these devices should be decoupled with low ESR 47 nF ceramic capacitors. Ground planes for both GND<sub>1</sub> and GND<sub>2</sub> are highly recommended for data rates above 10 Mbps. Capacitors must be located as close as possible to the V<sub>DD</sub> pins.

### Signal Status on Start-up and Shut Down

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.

### Data Transmission Rates

The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, those parameters which determine the limits of the data transmission are pulse width distortion and propagation delay skew.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high than when sending a high-to-low signal. This difference, or error, is called pulse width distortion (PWD) and is usually in nanoseconds. It may also be expressed as a percentage:

$$\text{PWD}\% = \frac{\text{Maximum Pulse Width Distortion (ns)}}{\text{Signal Pulse Width (ns)}} \times 100\%$$

For example, with data rates of 12.5 Mbps:

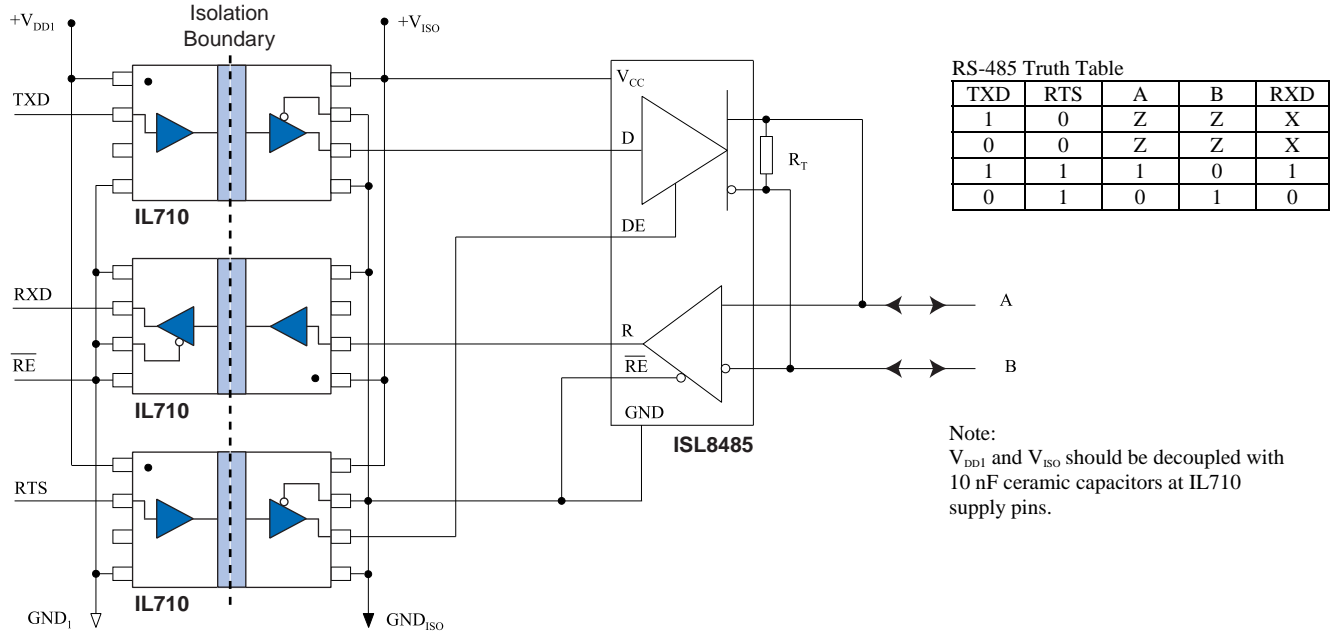
$$\text{PWD}\% = \frac{3 \text{ ns}}{80 \text{ ns}} \times 100\% = 3.75\%$$

This figure is almost **three times** better than any available optocoupler with the same temperature range, and **two times** better than any optocoupler regardless of published temperature range. IsoLoop isolators exceed the 10% maximum PWD recommended by PROFIBUS, and will run to nearly 35 Mb within the 10% limit.

Propagation delay skew is the signal propagation difference between two or more channels. This becomes significant in clocked systems because it is undesirable for the clock pulse to arrive before the data has settled. Short propagation delay skew is therefore especially critical in high data rate parallel systems for establishing and maintaining accuracy and repeatability. IL700 isolators have a maximum propagation delay skew of 6 ns, which is **five times** better than any optocoupler.

**Application Diagrams**

**Isolated PROFIBUS / RS-485**

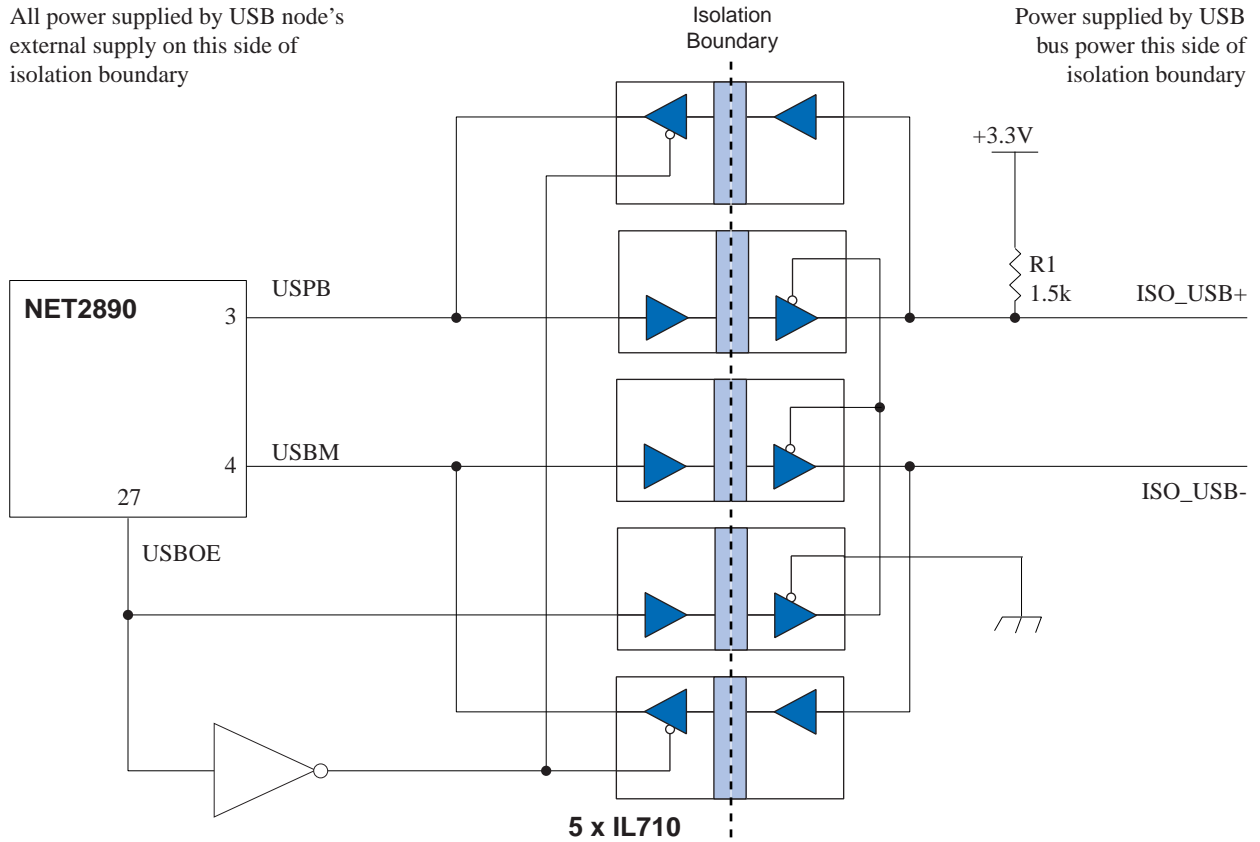


NVE offers a unique line of PROFIBUS/RS-485 transceivers, but IL710 isolators can also be used as part of multi-chip designs using non-isolated PROFIBUS transceivers.

**Isolated USB**

All power supplied by USB node's external supply on this side of isolation boundary

Power supplied by USB bus power this side of isolation boundary

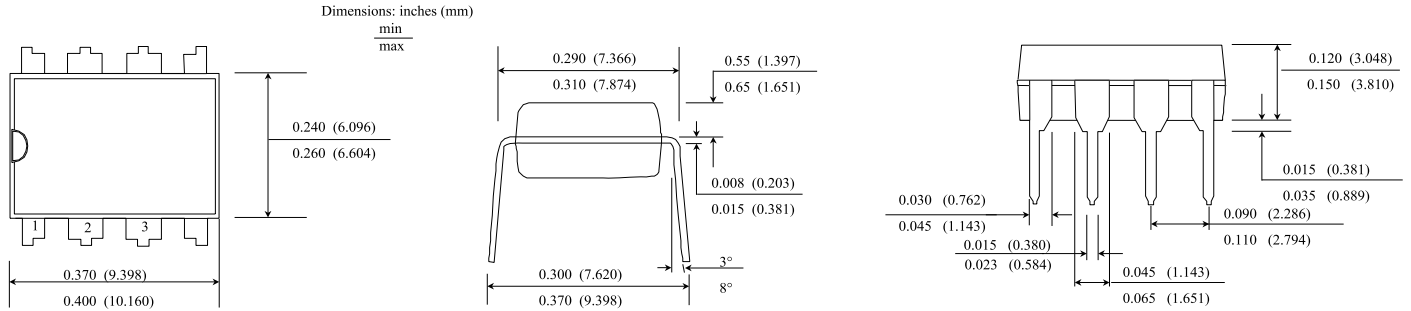


In this circuit, power is supplied by USB bus power on one side of the isolation barrier, and the USB node's external supply on the other side of the barrier. IL700 Isolators are specified at just 3 ns typical pulse width distortion.

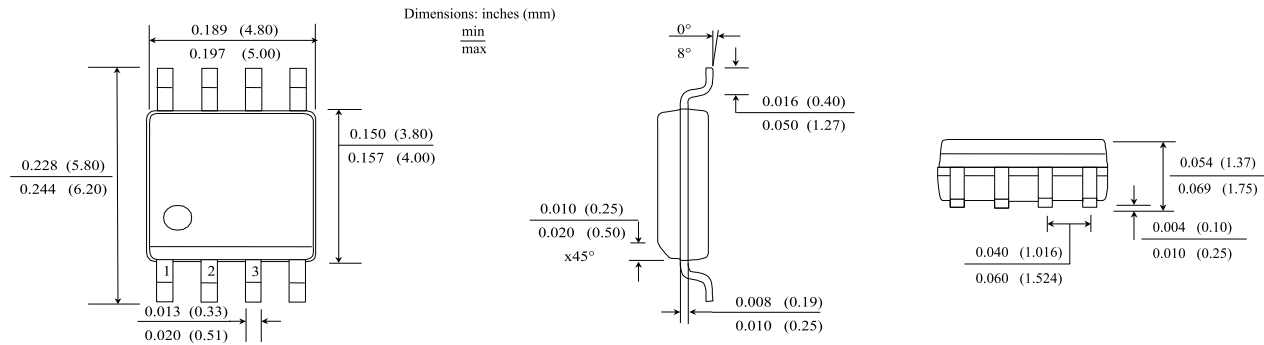


**Package Drawings, Dimensions and Specifications**

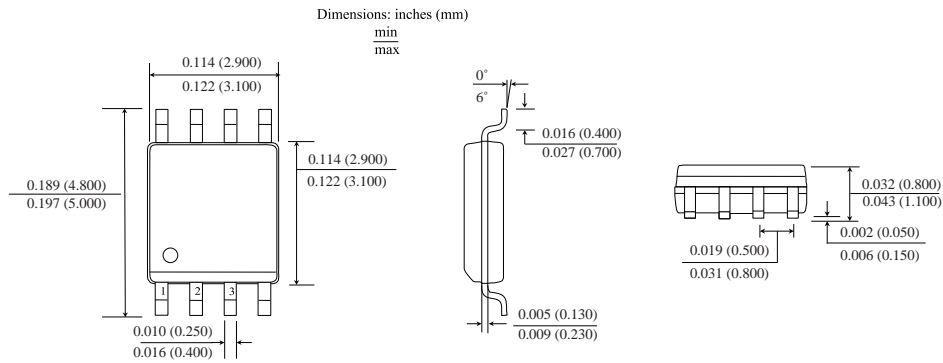
**8-pin PDIP Package**



**8-pin SOIC Package**

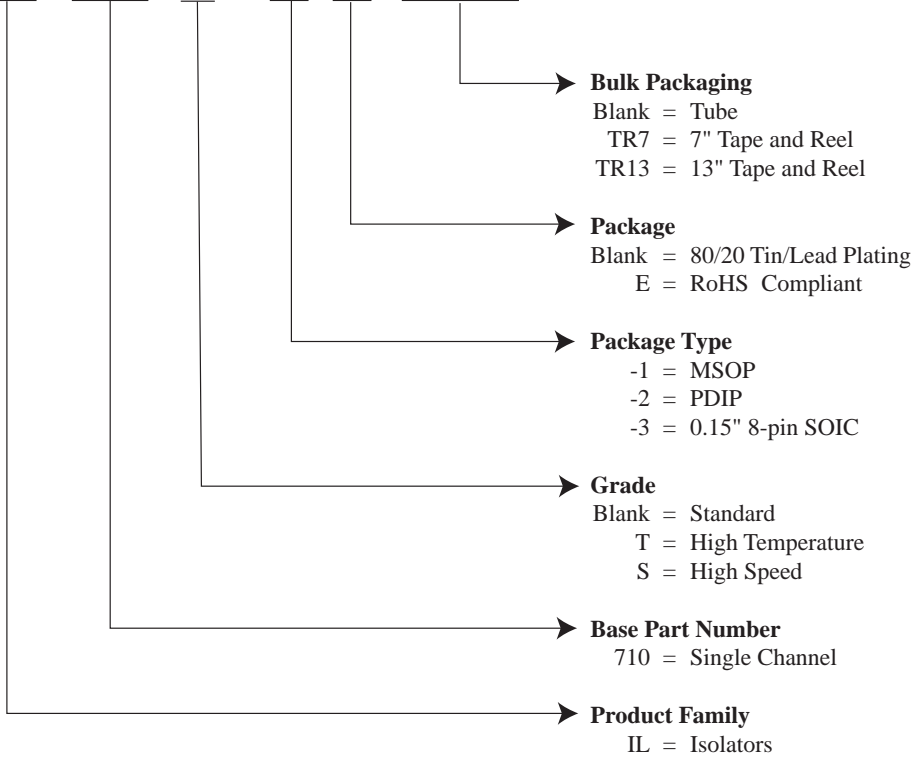


**8-pin MSOP Package**



**Ordering Information and Valid Part Numbers**

**IL 710 T - 3 E TR13**



**Valid Part Numbers**

IL710-1E  
 IL710S-1E  
 IL710T-1E

IL710-2  
 IL710T-2  
 IL710-2E  
 IL710T-2E

IL710-3  
 IL710S-3  
 IL710T-3  
 IL710-3E  
 IL710S-3E  
 IL710T-3E

All MSOP and SOIC parts are available on tape and reel.



**ISB-DS-001-IL710-M**  
**September 2007**

**Changes**

- Changed ordering information to reflect that devices are now fully RoHS compliant with no exemptions.

**ISB-DS-001-IL710-L**

**Changes**

- Eliminated soldering profile chart

**ISB-DS-001-IL710-K**

**Changes**

- Edited Profibus application

**ISB-DS-001-IL710-J**

**Changes**

- MSOP package, S- and T-Grades added
- Order information updated

**ISB-DS-001-IL710-I**

**Changes**

- Added MSOP specifications
- Updated UL and IEC numbers

**ISB-DS-001-IL710-H**

**Changes**

- Revision letter added.
- Storage temperature changed from 175°C max. to 150°C max.
- Lead soldering temperature changed from 180°C max. to 260°C max.
- Package Power Dissipation: Test Condition added:  $f = 1\text{MHz}$ ,  $V_{DD} = 5\text{V}$ .
- IEC 61010-1 Classification: “Reinforced Insulation” added.
- USB application circuit added.
- Ordering Information: 5 Volt only option removed.  
Valid Part Numbers IL710-2B, IL710-3B,  
IL710-2BE, and IL710-3BE removed.

## **About NVE**

An ISO 9001 Certified Company

NVE Corporation manufactures innovative products based on unique spintronic Giant Magnetoresistive (GMR) technology. Products include Magnetic Field Sensors, Magnetic Field Gradient Sensors (Gradiometers), Digital Magnetic Field Sensors, Digital Signal Isolators, and Isolated Bus Transceivers.

NVE pioneered spintronics and in 1994 introduced the world's first products using GMR material, a line of ultra-precise magnetic sensors for position, magnetic media, gear speed and current sensing.

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***Specifications are subject to change without notice.***

ISB-DS-001-IL710-M  
September 2007