

HD74LV374A

Octal Edge-Triggered D-type Flip-Flops with 3-state Outputs

REJ03D0332-0200Z
 (Previous ADE-205-275 (Z))
 Rev.2.00
 Jun. 25, 2004

Description

The HD74LV374A has eight edge trigger D type flip flops with three state outputs in a 20 pin package. Data at the D inputs meeting set up requirements, are transferred to the Q outputs on positive going transitions of the clock input. When the clock input goes low, data at the D inputs will be retained at the outputs until clock input returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- $V_{CC} = 2.0\text{ V to }5.5\text{ V}$ operation
- All inputs $V_{IH}(\text{Max.}) = 5.5\text{ V}$ (@ $V_{CC} = 0\text{ V to }5.5\text{ V}$)
- All outputs $V_O(\text{Max.}) = 5.5\text{ V}$ (@ $V_{CC} = 0\text{ V}$)
- Typical V_{OL} ground bounce $< 0.8\text{ V}$ (@ $V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.3\text{ V}$ (@ $V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Output current $\pm 8\text{ mA}$ (@ $V_{CC} = 3.0\text{ V to }3.6\text{ V}$), $\pm 16\text{ mA}$ (@ $V_{CC} = 4.5\text{ V to }5.5\text{ V}$)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV374AFPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)
HD74LV374ARPEL	SOP-20 pin (JEDEC)	FP-20DBV	RP	EL (1,000 pcs/reel)
HD74LV374ATELL	TSSOP-20 pin	TTP-20DAV	T	ELL (2,000 pcs/reel)

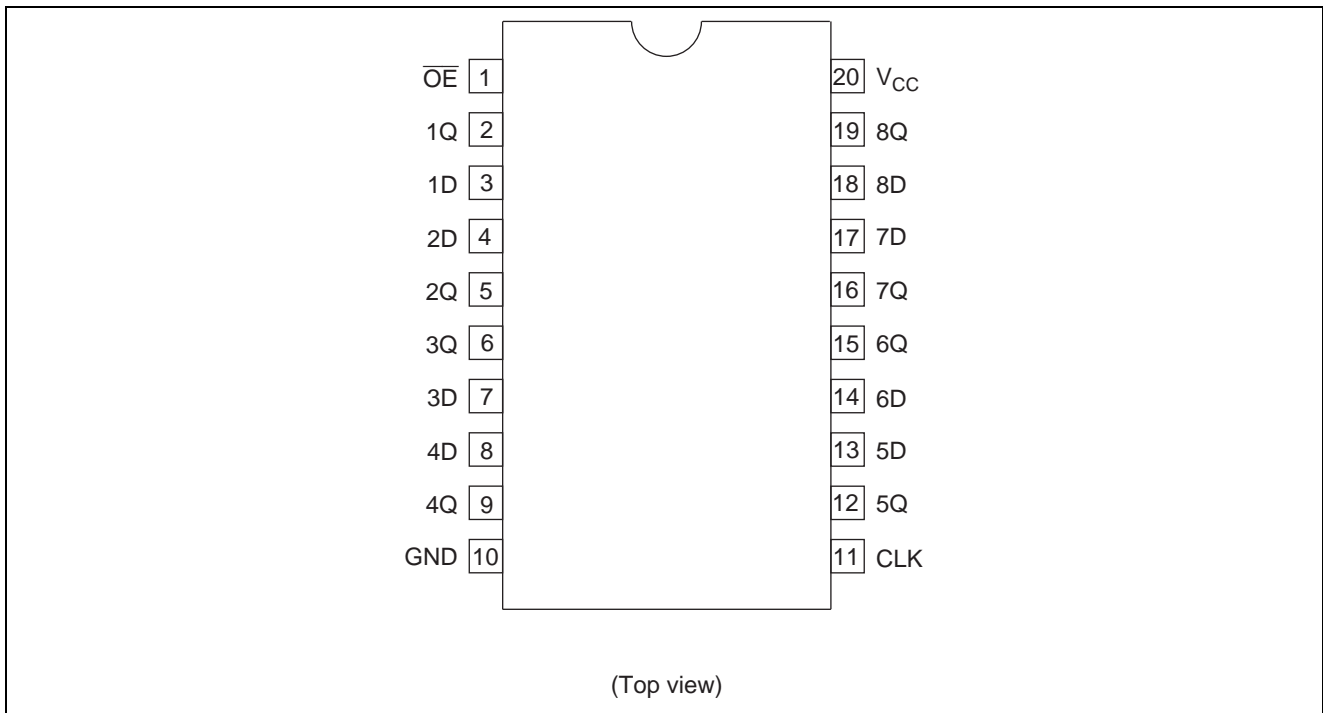
Note: Please consult the sales office for the above package availability.

Function Table

Inputs				Output Q
\overline{OE}	CLK	D		
H	X	X		Z
L	↑	L		L
L	↑	H		H
L	↓	X		Q_0

Note: H: High level
 L: Low level
 X: Immaterial
 Z: High impedance
 Q_0 : Output level before the indicated steady state input conditions were established.

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range ^{*1}	V_I	-0.5 to 7.0	V	
Output voltage range ^{*1, 2}	V_O	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output: H or L V_{CC} : OFF or Output: Z
Input clamp current	I_{IK}	-20	mA	$V_I < 0$
Output clamp current	I_{OK}	± 50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	± 35	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	± 70	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) ^{*3}	P_T	835 757	mW	SOP TSSOP
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

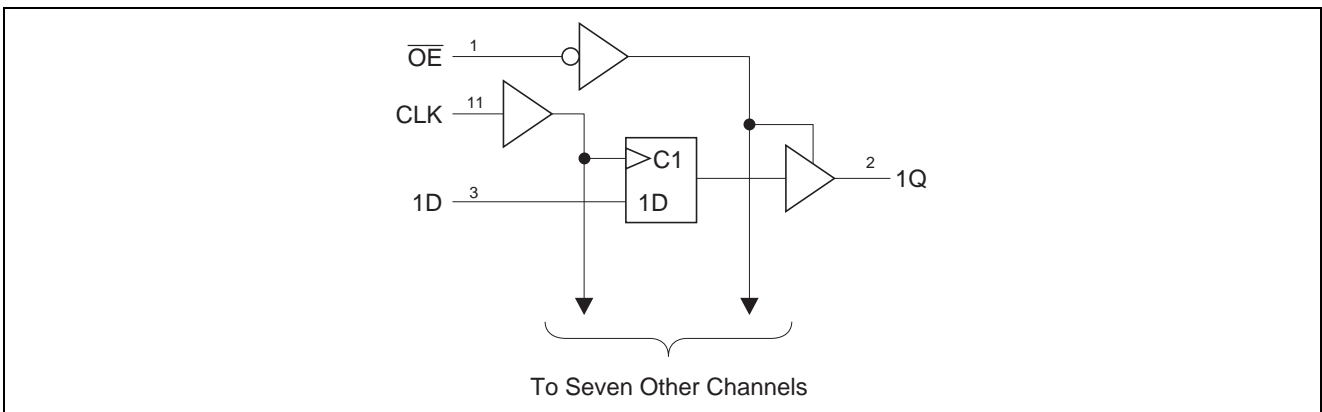
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	H or L
		0	5.5		High impedance state
Output current	I_{OH}	—	-50	μA	$V_{CC} = 2.0 V$
		—	-2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	-8		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	-16		$V_{CC} = 4.5 \text{ to } 5.5 V$
	I_{OL}	—	50	μA	$V_{CC} = 2.0 V$
		—	2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	8		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	16		$V_{CC} = 4.5 \text{ to } 5.5 V$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3 \text{ to } 2.7 V$
		0	100		$V_{CC} = 3.0 \text{ to } 3.6 V$
		0	20		$V_{CC} = 4.5 \text{ to } 5.5 V$
Operating free-air temperature	T_a	-40	85	$^{\circ}C$	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



DC Electrical Characteristics

Ta = -40 to 85°C

Item	Symbol	V _{CC} (V)*	Min	Typ	Max	Unit	Test Conditions		
Input voltage	V _{IH}	2.0	1.5	—	—	V			
		2.3 to 2.7	V _{CC} × 0.7	—	—				
		3.0 to 3.6	V _{CC} × 0.7	—	—				
		4.5 to 5.5	V _{CC} × 0.7	—	—				
	V _{IL}	2.0	—	—	0.5				
		2.3 to 2.7	—	—	V _{CC} × 0.3				
		3.0 to 3.6	—	—	V _{CC} × 0.3				
		4.5 to 5.5	—	—	V _{CC} × 0.3				
Output voltage	V _{OH}	Min to Max	V _{CC} - 0.1	—	—	V	I _{OH} = -50 μA		
		2.3	2.0	—	—		I _{OH} = -2 mA		
		3.0	2.48	—	—		I _{OH} = -8 mA		
		4.5	3.8	—	—		I _{OH} = -16 mA		
	V _{OL}	Min to Max	—	—	0.1		I _{OL} = 50 μA		
		2.3	—	—	0.4		I _{OL} = 2 mA		
		3.0	—	—	0.44		I _{OL} = 8 mA		
		4.5	—	—	0.55		I _{OL} = 16 mA		
	Input current	I _{IN}	0 to 5.5	—	—		±1	μA	V _{IN} = 5.5 V or GND
	Off-state output current	I _{OZ}	5.5	—	—		±5	μA	V _O = V _{CC} or GND
Quiescent supply current	I _{CC}	5.5	—	—	20	μA	V _{IN} = V _{CC} or GND, I _O = 0		
Output leakage current	I _{OFF}	0	—	—	5	μA	V _I or V _O = 0 to 5.5 V		
Input capacitance	C _{IN}	3.3	—	2.9	—	pF	V _I = V _{CC} or GND		

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

V_{CC} = 2.5 ± 0.2 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	t _{max}	60	105	—	50	—	MHz	C _L = 15 pF		
		50	85	—	40	—		C _L = 50 pF		
Propagation delay time	t _{PLH}	—	9.7	16.3	1.0	19.0	ns	C _L = 15 pF	CLK	Q
	t _{PHL}	—	11.8	19.3	1.0	23.0		C _L = 50 pF		
Enable time	t _{ZH}	—	8.9	15.9	1.0	19.0	ns	C _L = 15 pF	OE	Q
	t _{ZL}	—	10.9	18.8	1.0	22.0		C _L = 50 pF		
Disable time	t _{HZ}	—	6.3	12.6	1.0	15.0	ns	C _L = 15 pF	OE	Q
	t _{LZ}	—	8.2	17.3	1.0	19.0		C _L = 50 pF		
Setup time	t _{SU}	5.0	—	—	5.5	—	ns		Data before CLK ↑	
Hold time	t _H	2.5	—	—	2.5	—	ns		Data after CLK ↑	
Pulse width	t _w	6.0	—	—	7.0	—	ns		CLK: "H" or "L"	

V_{CC} = 3.3 ± 0.3 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	t _{max}	80	150	—	70	—	MHz	C _L = 15 pF		
		55	110	—	50	—		C _L = 50 pF		
Propagation delay time	t _{PLH}	—	6.8	12.7	1.0	15.0	ns	C _L = 15 pF	CLK	Q
	t _{PHL}	—	8.3	16.2	1.0	18.5		C _L = 50 pF		
Enable time	t _{ZH}	—	6.3	11.0	1.0	13.0	ns	C _L = 15 pF	OE	Q
	t _{ZL}	—	7.7	14.5	1.0	16.5		C _L = 50 pF		
Disable time	t _{HZ}	—	4.7	10.5	1.0	12.5	ns	C _L = 15 pF	OE	Q
	t _{LZ}	—	5.9	14.0	1.0	16.0		C _L = 50 pF		
Setup time	t _{SU}	4.5	—	—	4.5	—	ns		Data before CLK ↑	
Hold time	t _H	2.0	—	—	2.0	—	ns		Data after CLK ↑	
Pulse width	t _w	5.0	—	—	5.5	—	ns		CLK: "H" or "L"	

V_{CC} = 5.0 ± 0.5 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	t _{max}	130	205	—	110	—	MHz	C _L = 15 pF		
		85	170	—	75	—		C _L = 50 pF		
Propagation delay time	t _{PLH}	—	4.9	8.1	1.0	9.5	ns	C _L = 15 pF	CLK	Q
	t _{PHL}	—	5.9	10.1	1.0	11.5		C _L = 50 pF		
Enable time	t _{ZH}	—	4.6	7.6	1.0	9.0	ns	C _L = 15 pF	OE	Q
	t _{ZL}	—	5.5	9.6	1.0	11.0		C _L = 50 pF		
Disable time	t _{HZ}	—	3.4	6.8	1.0	8.0	ns	C _L = 15 pF	OE	Q
	t _{LZ}	—	4.0	8.8	1.0	10.0		C _L = 50 pF		
Setup time	t _{SU}	3.0	—	—	3.0	—	ns		Data before CLK ↑	
Hold time	t _H	2.0	—	—	2.0	—	ns		Data after CLK ↑	
Pulse width	t _w	5.0	—	—	5.0	—	ns		CLK: "H" or "L"	

Output-skew Characteristics

$C_L = 50 \text{ pF}$

Item	Symbol	$V_{CC} = (V)$	$T_a = 25^\circ\text{C}$		$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit
			Min	Max	Min	Max	
Output skew	$t_{sk(O)}$	2.3 to 2.7	—	2.0	—	2.0	ns
		3.0 to 3.6	—	1.5	—	1.5	
		4.5 to 5.5	—	1.0	—	1.0	

Note: Skew between any outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

Operating Characteristics

$C_L = 50 \text{ pF}$

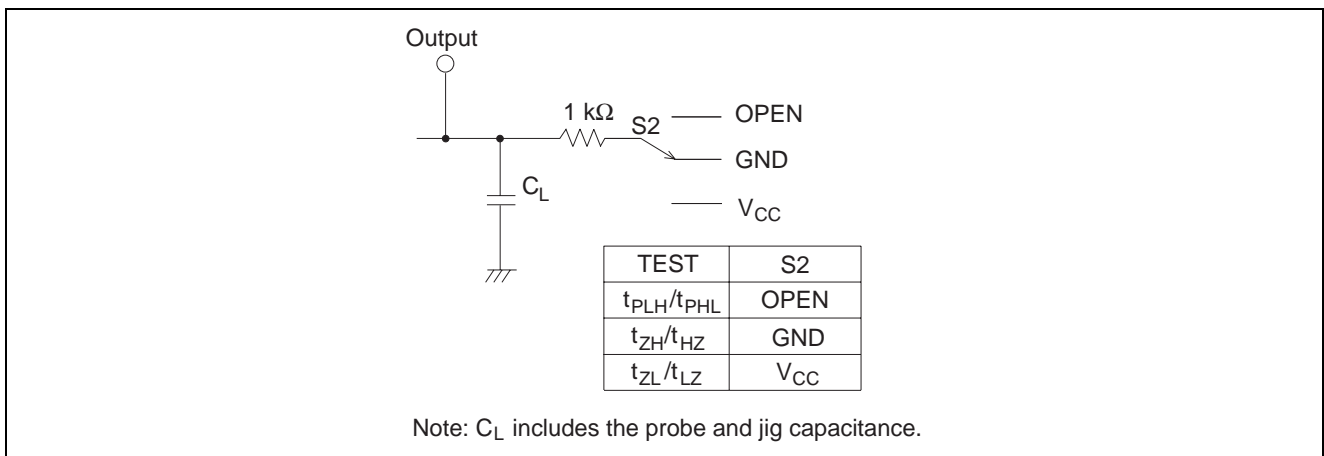
Item	Symbol	$V_{CC} = (V)$	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	3.3	—	21.1	—	pF	$f = 10 \text{ MHz}$
		5.0	—	22.8	—		

Noise Characteristics

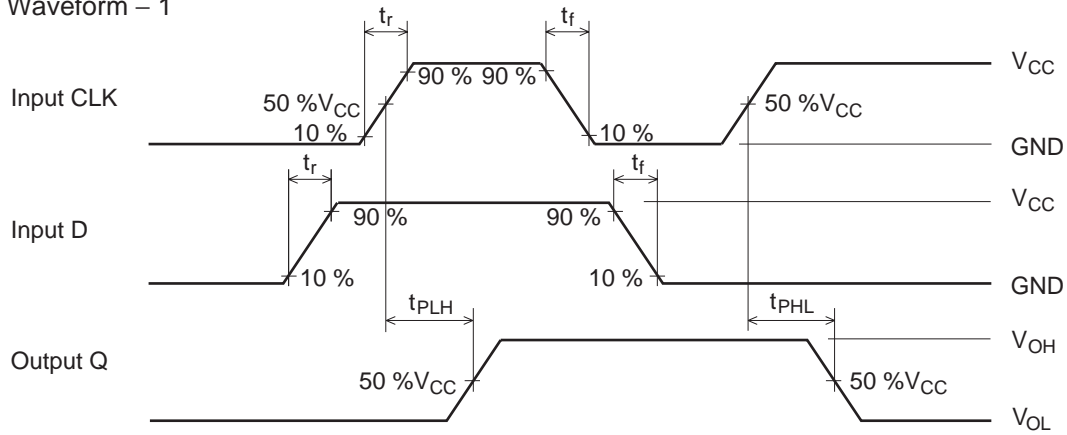
$C_L = 50 \text{ pF}$

Item	Symbol	$V_{CC} = (V)$	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$	3.3	—	0.6	0.8	V	
Quiet output, minimum dynamic V_{OL}	$V_{OL(V)}$	3.3	—	-0.5	-0.8	V	
Quiet output, minimum dynamic V_{OH}	$V_{OH(V)}$	3.3	—	2.9	—	V	
High-level dynamic input voltage	$V_{IH(D)}$	3.3	2.31	—	—	V	
Low-level dynamic input voltage	$V_{IL(D)}$	3.3	—	—	0.99	V	

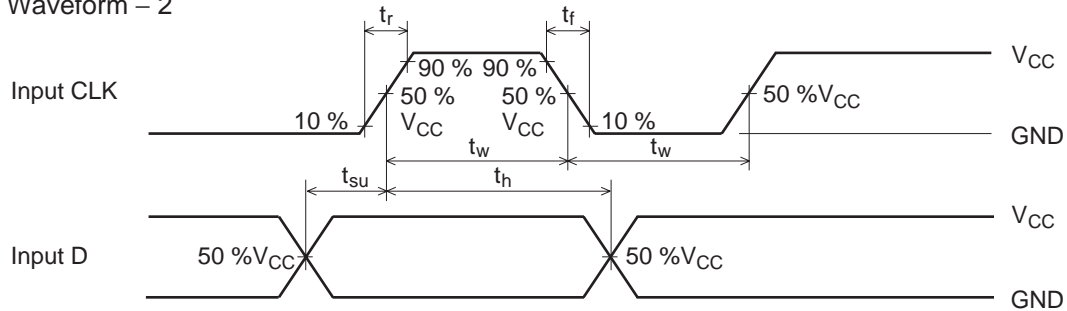
Test Circuit



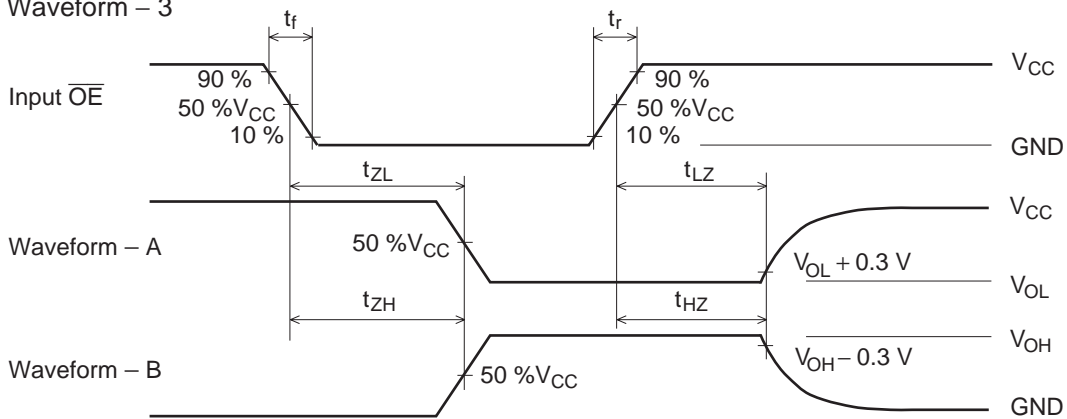
• Waveform – 1



• Waveform – 2

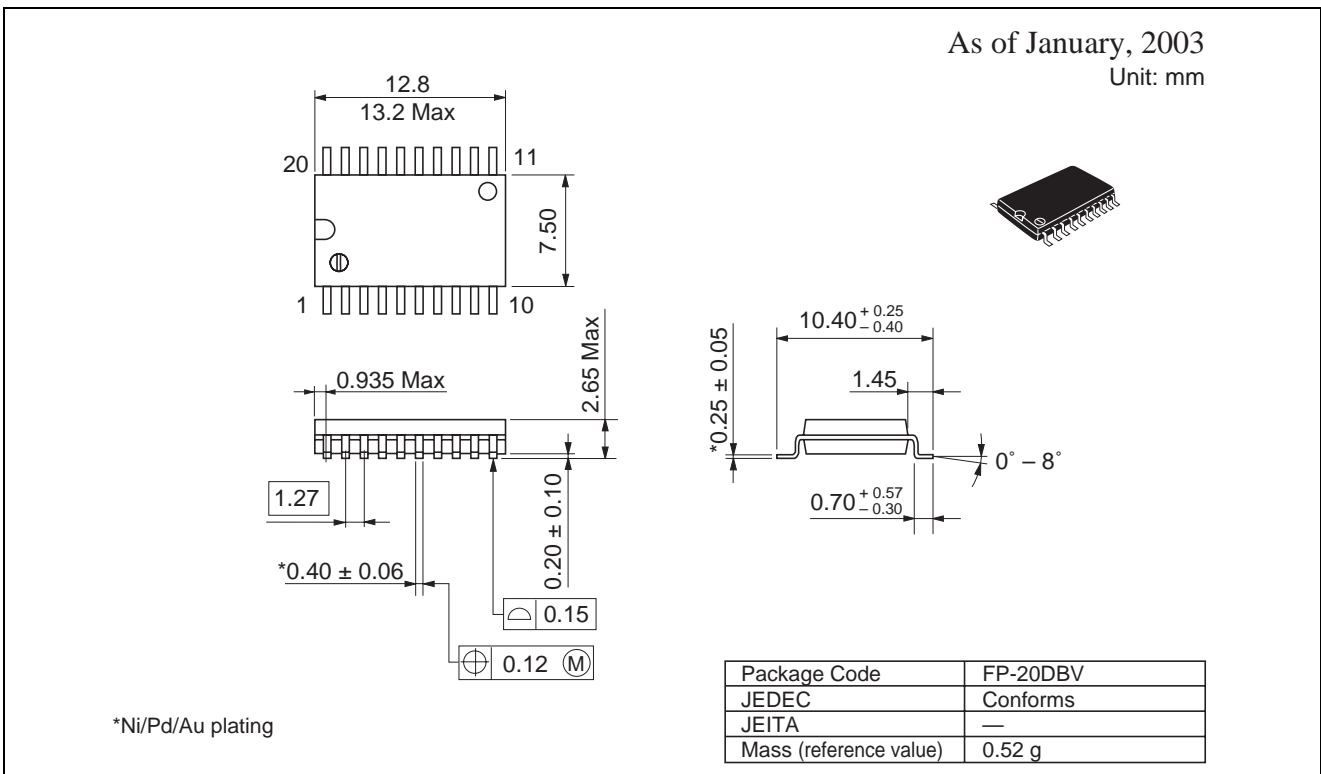
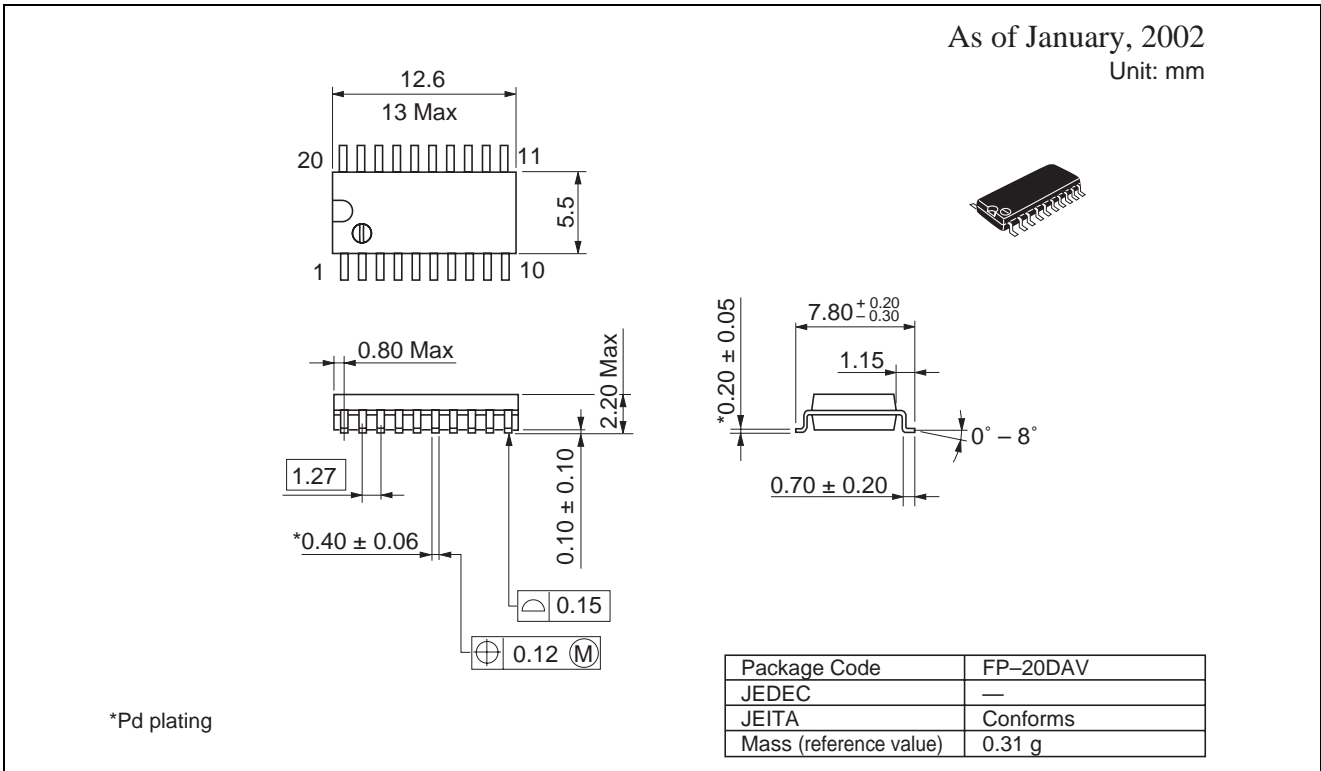


• Waveform – 3

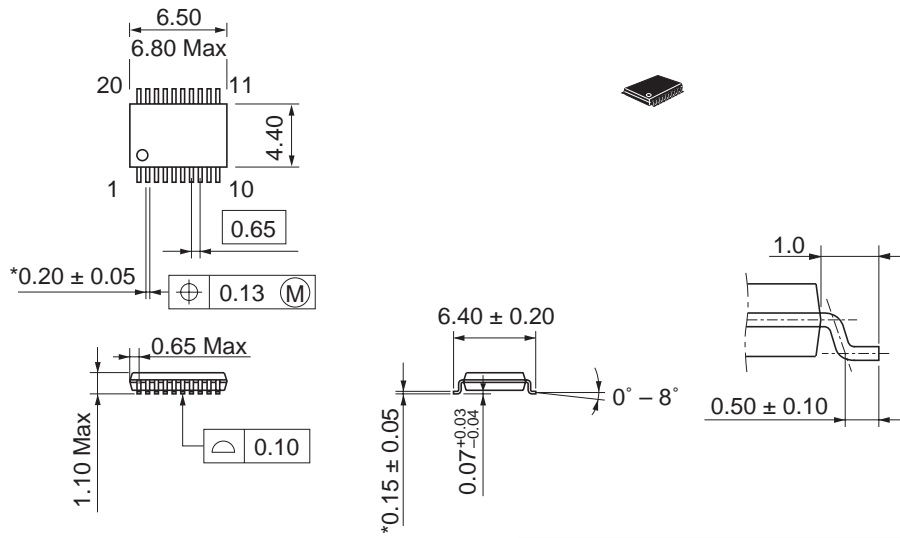


- Notes:
1. $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$
 2. Input waveform: PRR $\leq 1 \text{ MHz}$, duty cycle 50%
 3. Waveform-A is for an output with internal conditions such that the output is low except when disabled by the output control.
 4. Waveform-B is for an output with internal conditions such that the output is high except when disabled by the output control.

Package Dimensions



As of January, 2002
Unit: mm



*Pd plating

Package Code	TTP-20DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.07 g

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
 2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
 3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
 4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
 5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
 6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
 7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
 8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.
-



RENESAS SALES OFFICES

<http://www.renesas.com>

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH

Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.

7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.

FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

