DESCRIPTION

The MP020-5 is an offline, primary-side regulator that provides accurate constant voltage and constant current regulation without an opto-coupler or a secondary feedback circuit. It has an integrated 700V MOSFET.

The MP020-5's variable off-time control allows a flyback converter to operate in discontinuous conduction mode. The MP020-5 also features protection functions such as VCC under-voltage lockout, over-current protection, over-temperature protection, open circuit protection (OCP) and over-voltage protection. Its internal high-voltage start-up current source and power-saving technologies limit the no-load power consumption to less than 30mW.

The MP020-5's variable-switching-frequency technology provides natural spectrum shaping to smooth the EMI signature, making it suitable for offline, low-power battery chargers and adapters.

The MP020-5 is available in SOIC8-7A.

FEATURES

- Primary-Side–Control without Opto-Coupler or Secondary Feedback Circuit
- Precise Constant Current and Constant Voltage Control (CC/CV)
- Integrated 700V MOSFET with Minimal External Components
- Variable, Off-Time, Peak-Current Control
- 550µA High-Voltage Current Source
- 30mW No-Load Power Consumption
- Programmable Cable Compensation
- Multiple Protections: OVP, OCP, OCP, OTP, and VCC UVLO
- Natural Spectrum Shaping for Improved EMI Signature
- Low Cost and Simple External circuit
- SOIC8-7A Package

APPLICATIONS

- Cell Phone Chargers
- Adapters for Handheld Electronics
- Stand-By and Auxiliary Power Supplies
- Small Appliances

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

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ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number*</th>
<th>Package</th>
<th>Top Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP020-5GS</td>
<td>SOIC8-7A</td>
<td>MP020-5</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g. MP020-5GS–Z);

PACKAGE REFERENCE

ABSOLUTE MAXIMUM RATINGS (1)

Drain to GND .................................. -0.7V to 700V
VCC to GND ................................... -0.3V to 30V
CP to GND ..................................... -0.3V to 7V
FB Input ...................................... -0.7V to 10V
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC8-7A ...................................... 1.3W
Junction Temperature ......................... 150°C
Lead Temperature ............................. 260°C
Storage Temperature ......................... -60°C to +150°C
ESD Capability Human Body Mode ............ 2.0kV
ESD Capability Machine Mode ............... 200V

Recommended Operating Conditions (3)

Operating Junction Temp. (T_J) .......... -40°C to +125°C
Operating VCC range ......................... 6.6V to 28V

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_JA, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_JA. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
## ELECTRICAL CHARACTERISTICS

\( V_{CC} = 15V, T_A = 25°C, \) unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage Management (VCC Pin)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{CC} ) ON threshold</td>
<td>( V_{CCH} )</td>
<td></td>
<td>16.8</td>
<td>17.3</td>
<td>17.8</td>
<td>V</td>
</tr>
<tr>
<td>( V_{CC} ) OFF threshold</td>
<td>( V_{CCL} )</td>
<td></td>
<td>6</td>
<td>6.3</td>
<td>6.6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{CC} ) operating voltage</td>
<td></td>
<td></td>
<td>6.6</td>
<td>28</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Quiescent current</td>
<td>( I_Q )</td>
<td>At no load condition, ( V_{CC}=20V )</td>
<td></td>
<td>360</td>
<td>410</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Operating current</td>
<td>( I_{OP} )</td>
<td>60kHz, ( V_{CC}=20V )</td>
<td></td>
<td>500</td>
<td></td>
<td>( \mu A )</td>
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<tr>
<td>Leakage current from VCC Pin</td>
<td>( I_{Leak, VCC} )</td>
<td>( V_{CC}=0V \rightarrow 16V ), Drain float</td>
<td>0.1</td>
<td>1</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Internal MOSFET (Drain Pin)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Break-down Voltage</td>
<td>( V_{BRDSS} )</td>
<td>( V_{CC}=20V ), ( V_{FB}=7V )</td>
<td>700</td>
<td></td>
<td></td>
<td>V</td>
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<tr>
<td>Supply current from Drain Pin</td>
<td>( I_{Charge} )</td>
<td>( V_{CC}=4V ), ( V_{Drain}=100V )</td>
<td>450</td>
<td>550</td>
<td>750</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Leakage current from Drain Pin</td>
<td>( I_{Leak, Drain} )</td>
<td>( V_{DS}=500V_{DC} )</td>
<td>1</td>
<td>10</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>On-state resistance</td>
<td>( R_{ON} )</td>
<td>( I_D=10mA ), ( T_J=20°C )</td>
<td>10</td>
<td>13</td>
<td></td>
<td>( \Omega )</td>
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<tr>
<td>Minimum switching frequency</td>
<td>( f_{MIN} )</td>
<td>At no load condition</td>
<td>120</td>
<td></td>
<td></td>
<td>Hz</td>
</tr>
<tr>
<td>Internal Current Sense</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current limit</td>
<td>( I_{Limit} )</td>
<td>( V_{FB}=-0.5V )</td>
<td>365</td>
<td>380</td>
<td>395</td>
<td>mA</td>
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<tr>
<td>Leading-edge blanking</td>
<td>( t_{LEB} )</td>
<td></td>
<td>230</td>
<td>300</td>
<td>370</td>
<td>ns</td>
</tr>
<tr>
<td>Feedback input (FB Pin)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FB pin input current</td>
<td>( I_{FB} )</td>
<td>( V_{FB}=4V ), ( V_{CP}=3V )</td>
<td>12</td>
<td>16</td>
<td>20</td>
<td>( \mu A )</td>
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<tr>
<td>Feedback threshold</td>
<td>( V_{FB} )</td>
<td></td>
<td>3.93</td>
<td>4</td>
<td>4.07</td>
<td>V</td>
</tr>
<tr>
<td>DCM detect threshold</td>
<td>( V_{DCM} )</td>
<td></td>
<td>80</td>
<td>120</td>
<td>160</td>
<td>mV</td>
</tr>
<tr>
<td>FB open-circuit threshold</td>
<td>( V_{FBOPEN} )</td>
<td></td>
<td>-0.22</td>
<td>-0.15</td>
<td>-0.08</td>
<td>V</td>
</tr>
<tr>
<td>FB OVP threshold</td>
<td>( V_{FBOVP} )</td>
<td></td>
<td>6.2</td>
<td>6.35</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>OVP sample delay</td>
<td>( t_{OVP} )</td>
<td></td>
<td>3.5</td>
<td></td>
<td></td>
<td>( \mu s )</td>
</tr>
<tr>
<td>Output Cable Compensation (CP Pin)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cable compensation voltage</td>
<td>( V_{CP} )</td>
<td>Full load</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Thermal Shutdown</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal shutdown threshold</td>
<td></td>
<td></td>
<td></td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Thermal shutdown recovery threshold</td>
<td></td>
<td></td>
<td></td>
<td>120</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>
TYPICAL CHARACTERISTICS

Charge Current vs. Junction Temperature

Leakage Current vs. Junction Temperature

Breakdown Voltage vs. Junction Temperature

VCC ON Threshold vs. Junction Temperature

VCC OFF Threshold vs. Junction Temperature

Feedback Threshold vs. Junction Temperature

DCM Detect Threshold vs. Temperature Chart

FB Open Circuit Threshold vs. Junction Temperature

FB OVP Threshold vs. Junction Temperature
TYPICAL CHARACTERISTICS (CONTINUED)

- **OVP Sample Delay vs. Junction Temperature**
- **On State Resistance vs. Junction Temperature**
- **Current \( I_{\text{Limit}} \) vs. Junction Temperature**

![Graphs showing OVP sample delay, on state resistance, and current limit vs. junction temperature.](image-url)
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section. $V_{IN} = 230\text{Vac}, V_{OUT} = 5\text{V}, I_{OUT}=1\text{A}, L = 1.6\text{mH}, T_A = 25^\circ\text{C},$ unless otherwise noted.

- **Input Power Startup**
- **Input Power Shut Down**
- **OCkP Entry**
- **OCkP Recovery**
- **OVP Entry**
- **OVP Recovery**
- **Output Voltage Ripple**
- **Load Transient**
- **Normal Operation**
TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)
Performance waveforms are tested on the evaluation board of the Design Example section. 
\( V_{\text{IN}} = 230\text{VAC}, \ V_{\text{OUT}} = 5\text{V}, \ I_{\text{OUT}} = 1\text{A}, \ L = 1.6\text{mH}, \ T_A = 25^\circ\text{C}, \) unless otherwise noted.

MP020-5 CV/CC Characteristic
## PIN FUNCTIONS

<table>
<thead>
<tr>
<th>SOIC8-7A Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td>Supply. IC begins functioning when V\textsubscript{CC} charges to V\textsubscript{CCCH} through an internal high-voltage current source. When V\textsubscript{CC} falls below V\textsubscript{CCCL}, the internal high-voltage current source turns on to charge V\textsubscript{CC}. Connect 0.1\textmu F decoupling ceramic capacitor for most applications.</td>
</tr>
<tr>
<td>3</td>
<td>FB</td>
<td>Feedback. Provides the output reference voltage and detects falling voltage edges to determine the operation mode (CV mode and CC mode).</td>
</tr>
<tr>
<td>4</td>
<td>CP</td>
<td>Output Cable Compensation. Connect a 1\textmu F ceramic capacitor as a low pass filter. The upper resistor of resistor divider connected to FB adjusts the compensation voltage.</td>
</tr>
<tr>
<td>2, 5, 6</td>
<td>GND</td>
<td>Ground.</td>
</tr>
<tr>
<td>8</td>
<td>Drain</td>
<td>Internal MOSFET Drain. Input for the high-voltage start-up current source.</td>
</tr>
</tbody>
</table>
FUNCTIONAL BLOCK DIAGRAM

Figure 1: Functional Block Diagram
OPERATION

Figure 2: Simplified Flyback Converter

Startup
Initially, the IC is self-supplying through the internal high-voltage current source, which is drawn from the Drain pin. The internal high-voltage current source will turn off for better efficiency when \( V_{CC} \) reaches the \( V_{CC \ ON} \) threshold. Then the transformer’s auxiliary winding takes over as the power source. When \( V_{CC} \) falls below the \( V_{CC \ OFF} \) threshold, the IC stops switching and the internal high-voltage current source turns on again. See Figure 3 for the start-up waveform.

Working Principle
After startup, the internal MOSFET turns on and the current sense resistor (\( R_{CS} \)) senses the primary current \( i_P(t) \) internally. The current rises linearly at a rate of:

\[
\frac{di_P(t)}{dt} = \frac{V_{IN}}{L_M}
\]

As illustrated in Figure 4, when \( i_P(t) \) rises up to \( I_{PK} \), the internal MOSFET turns off. Then, the energy stored in the inductor transfers to secondary-side through the transformer.

The inductor, \( L_M \), stores energy with each cycle as a function of:

\[
E = \frac{1}{2} L_M \times I_{PK}^2
\]

So the power transferred from the input to the output is:

\[
P = \frac{1}{2} L_M \times I_{PK}^2 \times f_S
\]

Where \( f_S \) is the switching frequency. When \( I_{PK} \) is constant, the output power depends on \( f_S \).

Constant-Voltage Operation
The MP020-5 detects the auxiliary winding voltage from the FB pin and operates in constant voltage (CV) mode to regulate the output voltage.

Assume the secondary winding is the master and the auxiliary winding is the slave. When the secondary-side diode turns on, the FB pin voltage is:
\[ V_{FB} = \frac{N_{PAU}}{N_S} \times (V_O + V_D) \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}} \]

Where

- \( V_D \) is the secondary-side-diode forward-drop voltage,
- \( V_O \) is the output voltage,
- \( N_{PAU} \) and \( N_S \) are the number of auxiliary winding and secondary side winding turns (respectively), and
- \( R_{UP} \) and \( R_{DOWN} \) are the resistor-divider for sampling.

The output voltage differs from the secondary voltage due to the current-dependant forward-diode voltage drop. If the secondary voltage is always detected at a fixed secondary current, the difference between the output voltage and the secondary voltage is a fixed \( V_D \). The MP020-5 samples the auxiliary winding voltage 3.5\( \mu \)s after the primary switch turns off. The CV loop control function turns the secondary side diode off to regulate the output voltage.

**Constant Current Operation**

Figure 6 shows the constant-current operation.

\[ I_O \text{ estimator} \]

\[ ZCD \text{ Sample} \]

\[ V_{FB} \]

\[ V_{ZCD} \]

\[ V_{COMP_I} \]

\[ I_{O \text{ REF}} \]

\[ I_{PK} \]

The flyback always works in DCM, and the ZCD sample block can detect the duty cycle of the secondary-side diode.

In constant current (CC) operation, the product of \( V_{ZCD} \) and \( I_{pk} \) approximately equals \( I_{O \text{ REF}} \):

\[ I_{O \text{ REF}} = V_{ZCD} \times I_{pk} \]

So, the calculated output current from the \( I_O \) estimator block compares with reference value, \( I_{O \text{ REF}} \), and the error signal, \( V_{COMP_I} \), controls the turn on signal of the integral MOSFET. So \( I_O \) is then.

\[ I_O = \frac{1}{2} \times \frac{N_{PAU}}{N_S} \times I_{O \text{ REF}} \]

The MP020-5 maintains \( I_{O \text{ REF}} \) as 0.152A.

**Leading-Edge Blanking**

The parasitic capacitances induce a spike on the sense resistor when the power switch turns on. The MP020-5 includes a 300ns leading-edge blanking period to avoid falsely terminating the switching pulse. During this blanking period, the current sense comparator is disabled and the gate driver can not switch off. Figure 7 shows the leading-edge blanking.

**DCM Detection**

The MP020-5 operates in discontinuous conduction mode (DCM) in both CV and CC modes. To avoid operating in continuous conduction mode (CCM), the MP020-5 detects the falling edge of the FB input voltage with each cycle. If the chip does not detect a 120mV falling edge, it will stop switching.
OVP & OCkP
The MP020-5 includes over-voltage protection (OVP) and open-circuit protection (OCkP). If the voltage at the FB pin exceeds 6.35V for 3.5µs, or the FB input’s 0.15V falling edge cannot be monitored, the MP020-5 immediately shuts off the driving signals and enters hiccup mode. The MP020-5 resumes normal operation when the fault has been removed.

Thermal Shutdown (TSD)
When the temperature of the IC exceeds 150°C, over-temperature protection (OTP) triggers and the IC enters the auto recovery mode. When the temperature falls below 120°C, the IC will recover.

Output Cable Compensation
In order to compensate the secondary side cable voltage drop for a more precise output voltage, the MP020-5 has an internal output cable compensation circuit as shown in Figure 8. The internal ZCD sample can detect the duty of the secondary-side diode. A low-pass filter converts the duty signal to a DC voltage ($V_{CP}$) that changes as the load current varies.

$V_{CP}$ can be converted to a current signal drawn from the FB pin. The voltage drop on $R_{UP}$ helps the output cable compensation. When the system operates in maximum load, the CP pin voltage reaches a maximum of 2V.

$$V_{FCP} = \frac{5.6 \times D_S \times 2 \times R_{UP} \times N_S}{N_{P_{AU}}};$$

Where:
- $V_{FCP}$ is the secondary-side compensation voltage drop,
- $D_S$ is the secondary-diode duty cycle in CC mode (0.4 for the MP020-5),
- $R_{UP}$ is the upper resistor of resistor divider,
- $N_S$ is the number of turns for the secondary-side transformer windings, and
- $N_{P_{AU}}$ is the number of transformer auxiliary winding turns.

![Figure 8: Output Cable Compensator](image)
APPLICATION INFORMATION

COMPONENT SELECTION

Input Filter
The input filter helps convert the AC input to a DC source through the rectifier. Figure 9 shows the input filter, and Figure 10 shows the typical DC bus voltage waveform.

![Input Filter Diagram](image)

**Figure 9: Input Filter**

If $V_{DC\text{min}}$ cannot satisfy this expression, increase the value of the input capacitors to increase the $V_{DC\text{min}}$.

Output Capacitor
Use low ESR or very low ESR output capacitors to meet the output voltage ripple requirement without using an LC post filter. In addition, using low ESR capacitors improves output voltage regulation and feedback voltage sampling at high temperatures or low temperatures. Use an output capacitor with an ESR lower than 100mΩ for better efficiency over non-low ESR output capacitors.

Output Diode
Use a Schottky diode because of its fast switching speed and low forward-voltage drop for better high or low temperature CV regulation and efficiency.

If the lower average efficiency (3% to 4%) is acceptable, replace the output diode could with a fast or ultra-fast diode to reduce costs. Be sure to readjust the resistor divider values to for the correct output voltage because of the forward voltage drop is higher than the Schottky diode’s.

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If the lower average efficiency (3% to 4%) is acceptable, replace the output diode could with a fast or ultra-fast diode to reduce costs. Be sure to readjust the resistor divider values to for the correct output voltage because of the forward voltage drop is higher than the Schottky diode’s.

Leakage Inductance
The transformer’s leakage inductance will decrease the system efficiency and affect the output current or voltage constant precision. Optimize the transformer structure to minimize the leakage inductance. Aim for a leakage inductance less than 5% of the primary inductance.

**Leakage Inductance**

RCD Snubber
The transformer’s leakage inductance causes the MOSFET drain voltage to spike and the excessive ringing on the drain voltage waveform, which affects the output voltage sampling 3.5µs after the MOSFET turns off.

The RCD snubber circuit can limit the Drain voltage spike. Figure 11 shows the RCD snubber circuit.
Select $R_{SN}$ and $C_{SN}$ to meet the voltage spike requirements and improve system operation.

The power dissipated in the snubber circuit is approximately:

$$P_{SN} = \frac{1}{2} L_K \cdot I_{PK}^2 \cdot \frac{V_{SN}}{V_{SN} - N_{PS} \cdot V_O} \cdot f_S$$

Where:

- $L_K$ is the leakage inductance,
- $V_{SN}$ is the clamp voltage, and
- $N_{PS}$ is the turn ratio of primary and secondary side.

Since $R_{SN}$ consumes the majority of the power, $R_{SN}$ is approximately:

$$R_{SN} = \frac{V_{SN}^2}{P_{SN}}$$

The maximum ripple of the snubber capacitor voltage is then:

$$\Delta V_{SN} = \frac{V_{SN}}{C_{SN} \cdot R_{SN} \cdot f_S}$$

Generally, 15% ripple is reasonable, So the previous equation can estimate $C_{SN}$.

Normally, select a time constant ($\tau=R_{SN} \cdot C_{SN}$) less than 0.1ms for better CV sampling. Therefore, adjust the resistor based on the power loss and the acceptable clamp voltage in practical applications.

The damping resistor in series with the RCD has a relatively large value to prevent any excessive voltage ringing that can affect the CV sampling and increase the output ripple. Use a damping resistor value in the range of 200Ω to 500Ω to restrain the drain-voltage ringing.

### Divided Resistor

For better application performance, the select the resistor divider values from 10kΩ to 100kΩ to limit noise from adjacent components on the FB pin. If necessary, use a resistor between 1kΩ and 2kΩ connected between the FB pin and resistor divider limit substrate-injection-current effects, as shown in Figure 12.

For more accurate CV regulation, the accuracy of these feedback resistors should be at least 1%.

### Dummy Load

When system operates without any load and no dummy load, the output voltage will rise above normal operation because of the minimum switching frequency limitation. Use a dummy load for good load regulation. A large dummy load will deteriorate efficiency and no-load consumption, so the dummy load is tradeoff between efficiency and load regulation. For most applications, use a dummy load of around 10mW as it also satisfies the 30mW requirement.

### Maximum Switching Frequency

Use a secondary-side diode conduction time that exceeds 5.4µs, as per the following equation.
For high- or low-temperature applications, select a maximum switching frequency below 75kHz.

**PCB Layout Guide**

PCB layout is very important to achieve reliable operation, good EMI, and good thermal performance. The following describe some layout recommendations.

1. Minimize the loop area formed by the input capacitor, the MP020-5 drain-source, and the primary winding to reduce EMI noise.
2. The copper area connected to GND pins is the heat conduction path for the MP020-5. Provide at least 1 in$^2$ of top-side copper for adequate heat-sinking.
3. Minimize the clamp circuit loop to reduce EMI.
4. Minimize the secondary loop area of the output diode and output filter to reduce EMI noise. In addition, sufficient copper area should be provided at the anode and cathode terminal of the output diode to act as a heat sink.
5. Place the AC input away from the switching nodes to minimize the noise coupling that may bypass the input filter.
6. Place the bypass capacitor as close as possible to the IC and source.
7. Place the feedback resistors next to the FB pin and minimize the feedback sampling loop to minimize noise coupling.
8. Use a single point connection at the negative terminal of the input filter capacitor for the MP020-5 source pin and bias winding return.

Figure 13 shows a sample layout.

### Design Example

Below is a design example following the application guidelines based on these specifications:

<table>
<thead>
<tr>
<th>$V_{IN}$</th>
<th>85Vac~265Vac</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OUT}$</td>
<td>5V</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>1A</td>
</tr>
<tr>
<td>$f_S$</td>
<td>60kHz</td>
</tr>
</tbody>
</table>

Figure 14 shows the detailed application schematic. This circuit was used for the typical performance and circuit waveforms. For more device applications, please refer to the related evaluation board datasheets.

The transformer structure used in figure 14 could be benefit to pass the 3 wire Conducted
EMI (Output GND connect to earth) without Y cap. The Y cap will bring about the leakage current which is prohibited in some cell phone charger application. Figure 15 could illustrate how the Common Noise of the secondary side diode be restrained. The secondary side winding split to two separate windings $N_{SEC1}$ and $N_{SEC2}$ which have same turns and approximate parasitic capacitor $C_{SP1}$ and $C_{SP2}$ but their ‘hot spot’ is opposite as the Point 9 and Point 10 in Figure 15, so the common mode noise current produced at secondary side windings can be counteracted each other.

The transformer structure could be simple if the application does not need to pass the 3 wire Conducted EMI or could use the Y cap. Figure 16 shows the schematic with the simple transformer structure.
TYPICAL APPLICATION CIRCUITS

Figure 14: Typical Application, 5V/1A with Complicated Transformer Structure

Figure 15: Secondary Side Windings Structure to Restrain the Common Mode Noise
Figure 16: Typical Application, 5V/1A with Simple Transformer Structure
PACKAGE INFORMATION

SOIC8-7A

TOP VIEW

RECOMMENDED LAND PATTERN

FRONT VIEW

SIDE VIEW

DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE

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