

IDB-CI064-4021-XX-01

Overview

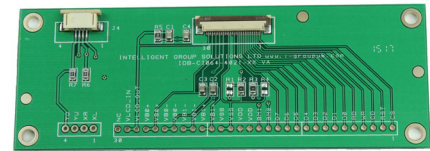
IDS have designed a break-out board for our CI064-4021-xx range of standard COG displays.

The IDB-CI064-4021-xx-01. enables our CI064-4021-xx COG displays to be used with a pin interface, and on the standard 0.1" header. The IDB-CI064-40721xx-01. Also has a built-in connector for a resistive touch screen option



LCD Connection

Insert the LCD Flexi with the white side up
 Push the brown Flexi Clamp Back in place



Touch Connector

Pin no	Symbol	Function
1	YD	Y axis down electrode
2	YU	Y axis up electrode
3	XR	X axis Right electrode
4	XL	X axis left electrode

Pin Description

Pin no	Symbol	Function
30	NC	No connection
29	VLCD_IN	Connected to VLCD_OUT pin for using internal DC/DC converter. When using LCD driving voltage, input the external VLCD voltage at this pin.
28	VLCD_OUT	Internal DC/DC converter output pin, need to connect a 330nF ~ 1.0uF capacitor between VSS and this pin for voltage decoupling. Leave this pin open when internal DC/DC converter is not used.
26-27	VB0+	LCD bias voltage are generated internally. Connect a 1uF ~ 2.2uF capacitors between VB1+ and VB1-, VB0+ and VB0-. Leave these pins open when internal DC/DC converter is not used.
24-25	VB0-	
22-23	VB1-	
20-21	VB1+	
19	VSS2	Ground (0V). Connect VSS, VSS2 together.
18	VSS	
17	VDD2	Power supply for VLCD, internal DC/DC Converter and other analog circuits. Keep the relationship of $VDD+1.3V \geq VDD2 \geq VDD$.
16	VDD	Power supply for display data RAM and digital logic (+3.3V)

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14	BM0	Bus mode : The interface bus mode is determined by BM[1:0] and {D7, D6} by following relationship.																																													
6-13	D0 ~ D7	Bi-directional bus for both serial and parallel interfaces. In serial mode, D0 = SCK, D3= SDA. The relationship is per below table.																																													
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4	WRO	WR[1:0] control the read/write operation of the interface type per below table																																													
3	CD	Display/control data select "H":display data ; "L":control data																																													
2	RST	External reset pin, low active																																													
1	CS0	When in parallel or SPI mode, served as chip select pin, low active When in I2C mode, served as A2 of slave address pin (A3/CS1=H, internally tied to VDD).																																													
A	LED+	Anode of LED backlight																																													
K	LED-	Cathode of LED backlight (0V)																																													